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AERO · SOFTWARE STACK RELEASE 2

Heterogeneous Computing for the European Cloud

An open, end-to-end software stack for the SiPearl Rhea processor and Arm / RISC-V hardware - from firmware and drivers up to GPU-accelerated AI, built entirely in open source.

THE FULL AERO SOFTWARE STACK

Open-source layers co-designed for the European Processor Initiative (EPI)



EU Cloud Services & Orchestration

Maestro · Knot · FaaSCell — serverless, FaaS & Kubernetes-native



Languages, Runtimes & Libraries

Quarkus · Mandrel · TornadoVM · GPULLama3.java · TeraHeap · LangChain4j



OS, Security & Heterogeneous Acceleration

Elastic Translations · VOSySmonitor · oneAPI Construction Kit (OCK) · SPIR-V · SYCL / DPC++



European Hardware

SiPearl Rhea (Arm Neoverse V1) · Arm Neoverse · RISC-V · GPU accelerators

3

pilots

9

real-world
use cases

VALIDATED ON

Ampere Altra · Graviton3 · Grace
(Arm Neoverse N1 · V1 · V2)

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UK Research
and Innovation



Schweizerische Eidgenossenschaft
Confédération suisse
Confederazione Svizzera
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Swiss Confederation

Federal Department of Economic Affairs,
Education and Research EAER
State Secretariat for Education,
Research and Innovation SERI

OS, Security & Heterogeneous Acceleration

The WP3 components that bring AERO up on Rhea - and their Release 2 results.

■ oneAPI Construction Kit (OCK) v5.0.0

OpenCL & SYCL driver for AArch64 CPUs — the acceleration foundation for the entire AERO stack.

- ▶ 100% OpenCL-CTS conformance on AArch64 · LLVM 20 / 21

■ Elastic Translations (Leshy)

Coalescing-aware, profiling-assisted huge-page promotion that targets MMU hotspots under fragmentation.

- ▶ +12–20% on memory-heavy workloads · –30% 2 MiB pages

■ VOSySmonitor

Arm TrustZone firmware enabling safe & secure mixed-criticality co-execution on Rhea.

- ▶ Validated on Arm FastModels for Rhea bring-up

■ Rhea Firmware & Drivers

Boot sequence and device drivers for the SiPearl Rhea platform.

- ▶ Integrated and validated via emulation

■ AXHEL — hardware-accelerated encryption

ARM aXceleration for Homomorphic Encryption: SVE / SVE2 modular-arithmetic kernels for Microsoft SEAL (CKKS).

- ▶ NTT, FMA & mod-mul kernels · Neoverse V2 gains over N1

100%

OpenCL-CTS on
AArch64 (OCK)

20%

faster (Elastic
Translations)

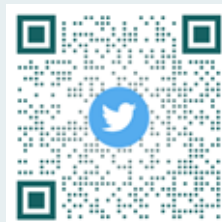
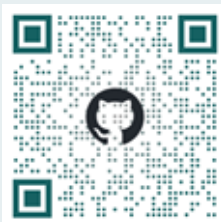
30%

fewer 2 MiB
pages (Leshy)

SVE2

accelerated
encryption (AXHEL)

Resources



Languages, Runtimes & Libraries

The WP4 components that program Arm & GPUs — and their Release 2 results.

■ TornadoVM v3.0.0

JIT-compiles Java to OpenCL, PTX & SPIR-V for CPUs and GPUs; now a full SDK.

► [Java 25](#) · [700+ tests](#) · [FP16 & tensors](#) · [RISC-V](#) · [SDKMAN!](#)

■ GPULLama3.java

GPU-accelerated LLM inference in pure Java; a Quarkus-LangChain4j provider.

► [7 GGUF model families](#) · [~73 tok/s on Grace Hopper](#)

■ TeraHeap

Adds a second, device-backed heap to OpenJDK's G1, cutting serialization cost.

► [Up to 45% faster Spark ML](#) · [26% Lucene](#) · [~97% SerDes](#)

■ SYCL / oneAPI (DPC++)

Cross-platform heterogeneous C++ on Arm via the OpenCL / SPIR-V path.

► [95.5% SYCL-CTS on Arm](#) · [AArch64 & RISC-V cross-compile](#)

■ Quarkus & Mandrel

Cloud-native Java with a faster GraalVM compiler and smaller runtimes.

► [GraalVM inliner +10%](#) · [JEP 493 upstreamed](#) · [JFR](#) · [Horreum](#)

■ LLVM Compiler Optimizations

CPU and GPU code-generation analyses and optimizations across the toolchain.

► [Improved vectorization & GPU codegen for AArch64](#)

45%

faster Spark ML
(TeraHeap)

73

tokens/s LLM
(GPULLama3)

32×

faster startup
(native)

95.5%

SYCL-CTS
on Arm

Resources



EU Cloud Services & Orchestration

The WP5 components for heterogeneous serverless & orchestration - and their results.

■ Maestro

Kubernetes-native orchestration, extended for heterogeneous hardware, serverless and Firecracker microVMs.

- Validated on GH200 (Arm) cluster + RISC-V k3s edge

■ Knative Serverless Controller

Migrated from JVM to Quarkus native for lightweight, fast and predictable serverless control.

- 32× faster startup (63.7 ms) · image 519 → 214 MB

■ FaaSCell

Firecracker snapshot-aware FaaS substrate developed in Rust that makes snapshotting a first-class orchestration concern (QoSnap).

- >99% of functions meet a 6× SLO at far lower memory

■ SnapBPF

eBPF snapshot-prefetching that captures and prefetches function working sets in kernel space.

- Beats REAP & FaaSnap · ported to Arm Neoverse V2

32×

faster cold-start
(native)

>99%

meet 6× SLO
(QoSnap)

2.4×

smaller image
(214 MB)

RISC-V

+ Arm, validated
at cloud & edge

Resources

